

Amendments to the claims:

1-4. (Cancelled)

5. (Currently Amended) A segmented digital to analog converter, comprising:
a first segment having a first plurality of resistors and configured to receive and convert
one set of digital bits of a digital input signal to an analog signal;
a second segment configured to receive and convert a second set of digital bits of the
input signal to an analog signal, the second segment having a second series of resistors
configured to receive the first set of digital bits, a first current source connected at one end of the
second series of resistors, and a second current source connected at another end of the second
series of resistors; and
a third segment having a third segmented series of resistors including a third set of
resistors connected end to end from along which an output can be generated at any point between
the resistors;

A segmented analog to digital converter of Claim 4, wherein the third segmented series of
resistors further includes one current source connected at one end of the third series of resistors,
and a second current source connected at another end of the third series of resistors.

6. (Currently Amended) A segmented analog to digital converter of Claim 5, 4,
wherein the third segmented series of resistors further includes one current source connected at
one end of the third series of resistors, and a second current source connected at another end of
the third series of resistors, and wherein the control of at least three current sources are
coordinated.

7. (Currently Amended) A segmented analog to digital converter of Claim 5, 4,
wherein the third segmented series of resistors further includes one current source connected at
one end of the third series of resistors, and a second current source connected at another end of
the third series of resistors, and wherein the control of at least three cascaded current sources
connected to each of the three segments are coordinated.

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8. (Currently Amended) A segmented analog to digital converter of Claim 5, 4, wherein the third segmented series of resistors further includes one current source connected at one end of the third series of resistors, and a second current source connected at another end of the third series of resistors, and wherein current is delivered from each of the three current sources connected to each of the three segments in a cascoded manner.

9. (Currently Amended) A segmented analog to digital converter of Claim 5, 4, wherein each of the three segmented series of resistors is connected to one set of cascaded current sources that provide current to one end of each series of resistors, and at another end to another set of cascaded current sources to provide current to another end of each series of resistors.

10. (Currently Amended) A segmented analog to digital converter of Claim 5, 4, wherein each of the three segmented series of resistors is connected at one end to one set of cascaded current sources to source current to one end of each series of resistors, and at another end to another set of cascaded current sources to draw current from another end of each series of resistors.

11. (Currently Amended) A segmented analog to digital converter of Claim 5, 4, further comprising at least one additional set of segmented series resistors, wherein each segmented series of resistors is connected to one set of cascaded current sources that provide current to one end of each series of resistors, and at another end to another set of cascaded current sources to provide current to another end of each series of resistors.

12. (Previously added) A segmented digital to analog converter, comprising: at least three segments that each have an individual plurality of resistors and configured as a set to receive and convert one set of digital bits of a digital input signal to an analog signal; wherein each segment is connected to one set of cascaded current sources that provide current to one end of each series of resistors, and is connected at another end to another set of cascaded current sources to provide current to another end of each series of resistors.

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13. (Previously added) A segmented digital to analog converter according to Claim 12, wherein at least two segments each include an individual segmented series of resistors that are each connected at segmented points to a switching circuit.

14. (Previously added) A segmented digital to analog converter according to Claim 12, wherein at least two segments each include an individual segmented series of resistors that are each connected at segmented points to a switching circuit, the converter further comprising additional successive segments of resistors connected one end to and receiving current from one set of cascaded current sources and further connected another end to and receiving current from another set of cascaded current sources.

15. (Previously added) A segmented digital to analog converter according to Claim 12, wherein at least two segments each include an individual segmented series of resistors that are each connected at segmented points to a switching circuit, the converter further comprising additional successive segments of resistors connected one end to and receiving current from one set of cascaded current sources connected to each other via an inverted gate connection and further connected another end to and receiving current from another set of cascaded current sources.